What is claimed is:

1- A probe assemblage for providing electrical connection simultaneously between one or more integrated circuits on a semiconductor wafer and a circuit test equipment, said assemblage including:

an interposer comprising a dielectric material having two major surfaces,

a plurality of protruding contact elements on one major surface of said interposer, each element corresponding to a test pad on one or more integrated circuits,

a plurality of conductive vias connecting each of said contact elements to a metallized pad on the second surface of said interposer,

a plurality of conductive leads fanning outward from said metallized pads to a standardized array of interposer connectors,

a compliant material underlying said contact elements on the first surface, and/or said interposer connectors on the second surface of the interposer,

a probe card having an array of connectors corresponding to said interposer connector array, and

means for attaching said probe card to said interposer.

2- An assemblage as in claim 1 wherein said protruding contact elements comprise a noble or oxide limiting metal.

3- An assemblage as in claim 1 wherein said protruding contact elements are stud bumps.

4- An assemblage as in claim 1 wherein said contact elements are microwires.

5- An assemblage as in claim 1 wherein the interposer has a coefficient of thermal expansion in the range of 2 to 10 PPM.

6- An assemblage as in claim 1 wherein said interposer includes one or more buried metal ground planes.

7- An assemblage as in claim 1 wherein said pads and connecting leads on the interposer comprise a first layer of copper and second layer of a laser ablatable material.

8- An assemblage as in claim 1 wherein said pads and connecting leads on the interposer are patterned by laser ablation in combination with chemical etching.

9- An assemblage as in claim 1 wherein the conductor pattern of leads and pads is software generated and input to a laser.

10- An assemblage wherein said chip contact elements are spaced more closely than the probe card connectors.

11- An assemblage as in claim 1 wherein said connectors on the second surface of the interposer mate to an array of connectors on a probe card.

12- An assemblage as in claim 1 wherein said connectors on the probe card are arrayed in a universal pattern common to multiple circuit devices.

13-An assemblage as in claim 1 wherein said means to attach the interposer to the probe card is a plurality of threaded machine screws.

14- An assemblage as in claim 1 wherein said means to attach the interposer to probe card is a cam ring locking mechanism.

15- An assemblage as in claim 1 including a source of ultrasonic energy coupled to said chip contact elements.

16- A probe assemblage for providing electrical connection between an integrated circuit chip on a semiconductor wafer and a circuit test equipment, said assemblage including:

an interposer comprising a dielectric material having two major surfaces and contoured sides of the interposer,

a plurality of protruding contact elements positioned atop a compliant material on one major surface of said interposer, each element corresponding to a test pads on the chip,

a plurality of conductive vias connecting each of said contact elements to a metallized pad and a standardized array of connectors on the second surface of said interposer,

a probe card having an array of connectors corresponding to said standardized contact array, and

means attaching said probe card to said interposer.

17- An assemblage as in claim 16 wherein said means to attach the probe card and interposer is by press fit.

18- A probe assemblage for providing electrical connection between an integrated circuit chip on a semiconductor wafer and a circuit test equipment, said assemblage including:

an interposer comprising a dielectric material having two major surfaces and contoured sides of said interposer and,

a plurality of protruding contact elements positioned atop a compliant material on one major surface of said interposer corresponding to test pads on the chip,

a plurality of conductive leads connecting each of said contact elements to a metallized pad and a standardized array of connectors on the second surface of said interposer,

a probe card having an array of connectors corresponding to said standardized connector array, and

said interposer is press fit into said probe card.

19- A test probe assemblage for simultaneously providing electrical connection between scribe line test structures on one or more integrated circuits on a semiconductor wafer and an electrical test equipment, said assemblage including:

an interposer comprising a dielectric material having two major surfaces,

a plurality of protruding contact elements positioned atop a compliant material on one major surface of said interposer corresponding to test pads on one or more integrated circuits,

a plurality of conductive vias connecting each of said contact elements to a metallized pad on the second surface of said interposer,

a plurality of leads fanning outward from said pads to a standardized array of connectors,

a probe card having an array of connectors corresponding to said standardized contact array, and

a means to attach said probe card to said interposer.

20- A method of forming an assemblage for simultaneously providing electrical connection between one or more integrated circuits on a semiconductor wafer and a circuit tester, including the following steps:

-providing an dielectric interposer having thermal expansion characteristics similar to that of silicon, and having a plurality of conductive vias at locations corresponding to the distance between chip contact pads which extending from the first major surface to the second major surface of the interposer,

-affixing a layer of highly conductive metal on each major surface,

-patterning an array of pads corresponding to chip contact pads on the first surface,

- patterning an array of pads at the via egress point on the second surface and an array of conductive leads terminating in a standardized pattern,

- bonding a chip contact element to each patterned contact pad on the first surface, and a connector element on the terminal of each lead on the second surface,

- providing a compliant material layer underlying the chip contact elements, and/or probe connector on the interposer,

- providing a probe card having a mating connector to that on said interposer, and

- aligning said connectors, and mechanically attaching.

21- A method as in claim 20 wherein said patterns on the interposer surface are software input to a computer controlled laser.

22- A method as in claim 20 wherein said metal patterns are formed by at least partially by laser ablation.

23- A method as in claim 20 wherein said metal patterns are formed by photolithography and chemical etching.